**Homework #4**

5 points each for the following questions.

1. Draw the logic diagram of the digit circuit specified by the following Verilog description:

(a)

**module** Circuit\_A (A, B, C, D, F);

**input** A, B, C, D;

**output** F;

**wire** w, x, y, z, a, d;

**or** (x, B, C, d);

**and** (y, a ,C);

**and** (w, z ,B);

and (z, y, A);

**or** (F, x, w);

**not** (a, A);

**not** (d, D);

**endmodule**

(b)

**module** Circuit\_B (y1, y2, y3, a, b);

**output** y1, y2, y3;

**input** a, b;

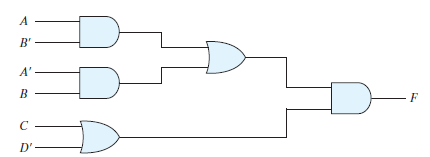
**assign** y1 = a || b;

**and** (y2, a, b);

**assign** y3 = a && b;

**endmodule**

1. (a) write a Verilog description of the circuit shown below



**module** Circuit (F, A, A\_bar, B, B\_bar, C, D\_bar);

**………..**

**endmodule**

(b) write a Verilog description of the circuit specified by the following Boolean function:

Z = (A + B’)C’(C + D)

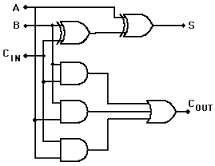
1. The adder-subtractor has the following values for mode input M and data inputs A and B:

M A B

1. 0 1100 1000
2. 1 0111 0110
3. 1 0000 0001
4. 0 0101 1010

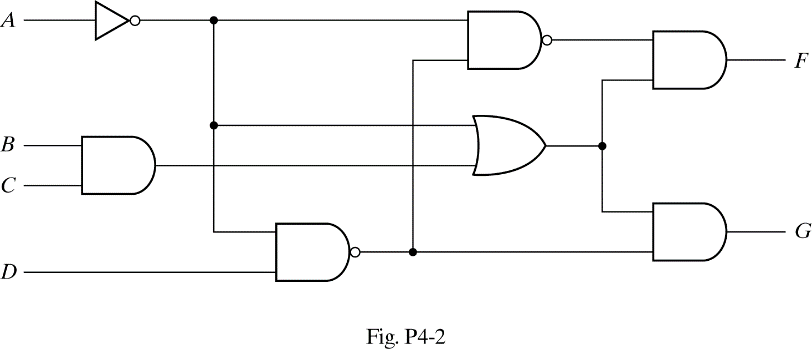
In each case, determine the values of the SUM outputs, the carry C, and overflow V.

1. Assume that the exclusive-OR gate has a propagation delay of 15ns and that the AND and OR gates have a propagation delay of 10 ns. (a) What is the propagation delay time of following 1-bit full adder?

 1-bit adder



1. Use Boolean theorems or K-maps to obtain the simplified Boolean expressions for outputs F and G in terms of the input variables in the following circuit.



1. Use 4 half-adders to design a four-bit combinational circuit increamenter (a circuit that adds 1 to a four-bit binary number). Draw the logic diagram.
2. Draw the logic diagram of a combinational circuit that compares two four-bit numbers if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise. (hint: XOR or XNOR gate can be used to check if two bits are equal).

**For the following circuit design questions (10 points each), you must show the procedure of obtaining the truth-table, obtaining the simplified logic function using k-map, and drawing logic diagram.**

1. (a) Design a half-subtractor circuit with inputs x and y and outputs Diff and Bout . The circuit subtracts the bits x – y and places the difference in D and the borrow in Bout.

(b) Design a full-subtractor circuit with three inputs x, y, Bin and two outputs Diff and Bout. The circuit subtracts x – y – Bin, where B in is the input borrow, Bout is the output borrow, and Diff is the difference.

1. Design a combinational circuit with three inputs, x, y and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is three less than the input.
2. Design a four-bit combinational circuit 2’s complementer. (The output generates the 2’s complement of the input binary number.)